

REMARKS

In the Amendment of January 20, 2005, proposed amendments to Fig. 19 were enclosed to overcome the objection of the Examiner.

Claims 1-4 were rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA), in view of Schilling et al., Electronic Circuits: Discrete and Integrated, 1979, pages 560-615.

In the Amendment of January 20, 2005, claims 1-4 were cancelled, without prejudice or disclaimer, and new claims 5-8 were substituted for claims 1-4 since claims 1-4 as amended in the Preliminary Amendment previously filed did not properly show all amendments made from the originally filed application. Once again, Applicant regrets any inconvenience or confusion caused.

Applicant respectfully submits that the rejections under 35 U.S.C. §112, second paragraph, made in the Office Action of October 20, 2004 were addressed in substituted new claims 5-8.

Independent claims 5, 6, and 8 were amended in the Amendment of January 20, 2005 to clarify that a test pattern is outputted by allowing only selected output buffers to change output values, thereby insuring that the total noise value is at most equal to an allowable noise value upon performing the output of the test pattern.

In contrast, in the Applicant's Admitted Prior Art (AAPA), the input pattern set in the scan cells as a test pattern for the internal circuit of the LSI is a fixed pattern, and the output buffers sequentially receive and output the data without simultaneously changing among the output buffers by the delay elements inserted between the scan cells and the output buffers.

In the Office Action of October 20, 2004, the Examiner acknowledges that AAPA fails to disclose a test pattern generating process that is "performed based on circuit component noise margin ... adjustments", and cites Schilling et al. as teaching well-known means for regulating fan-in and fan-out based on noise margins (see, e.g., FIGs. 12.1-3, 4 and pp 564, 565 of Schilling).

Applicant suggests that the cited portions of Schilling may be read to teach that, when an electronic circuit, such as a TTL circuit where an input current flow at an input gate is driven, a total input current at the driven TTL gate grows in proportion to circuit fan-out. As a result, the output voltage at a driver gate that drives the TTL gates decreases in proportion to fan-out decreases in proportion to fan-out when the driver gate output is high-level, and the output voltage at the driver gate that drives the TTL gates increases in proportion to fan-out when the driver gate output is low-level. In either case, the noise margin diminishes with fan-out. In essence, Schilling teaches adjustment of noise margin and fan-out requirements in the design of circuits having such performance characteristics.

In sharp contrast to Applicant's claimed invention, Schilling et al. in combination with AAPA does not teach Applicant's claimed method for reducing a noise in a power supply and ground that is generated from a momentary large current surge caused by simultaneous operation of output buffers. Schilling et al. provides no suggestion for the control noise values generated by output buffers.

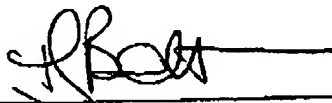
CLOSING

In view of the above amendments, it is believed that independent claims 5, 6, and 8 are in condition for allowance, as well as those claims dependent therefrom. Passage of this case to allowance is earnestly solicited.

However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper, not fully covered by an enclosed check, may be charged on Deposit Account 50-1290.

Respectfully submitted,


Thomas J. Bean
Reg. No. 44,528

CUSTOMER NO.: 026304

TELEPHONE NO.: (212) 940-8800
FAX NO.: (212) 940-8986/7
ATTORNEY DOCKET NO.: NEC 15.938A
TJB:td

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